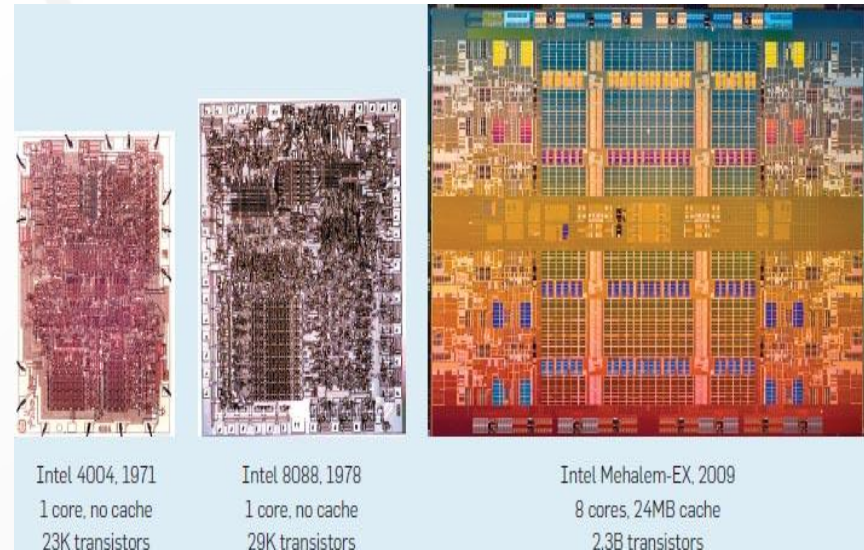
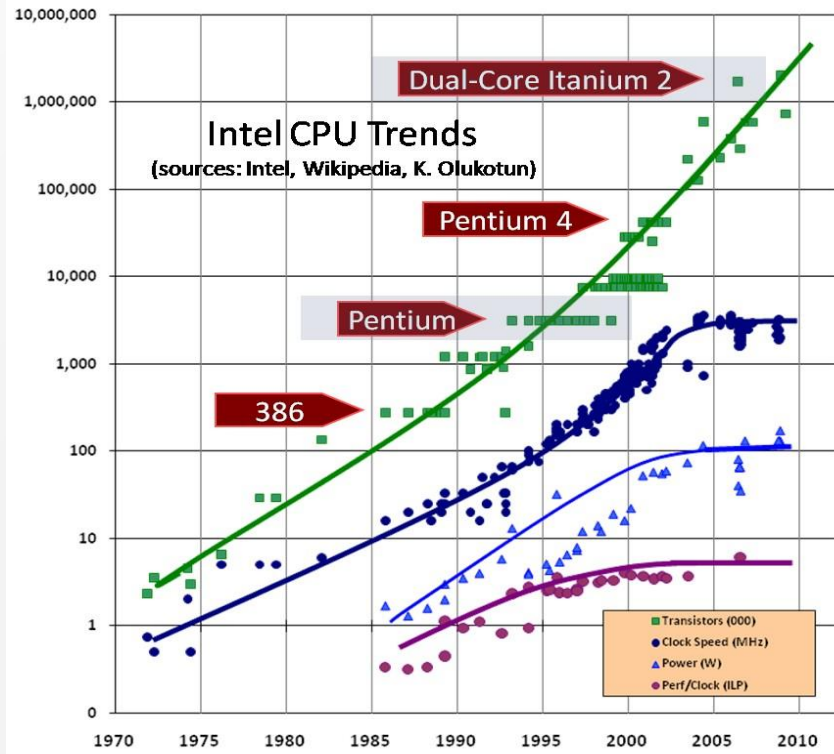




# 10x10 Heterogeneous Architecture with OpenDwarfs on FPGA

Anshuman Verma

# Power Wall and Multi core generation



# Dark Silicon

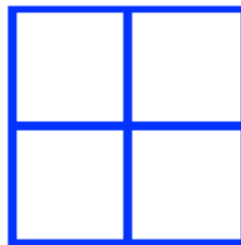
## Utilization Wall:

### Dark Silicon's Effect on Multicore Scaling

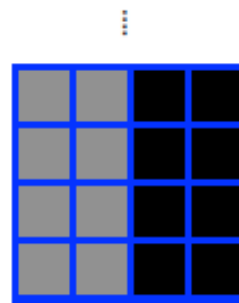
Spectrum of tradeoffs  
between # of cores and  
frequency

Example:  
65 nm  $\rightarrow$  32 nm ( $S = 2$ )

4 cores @ 1.8 GHz

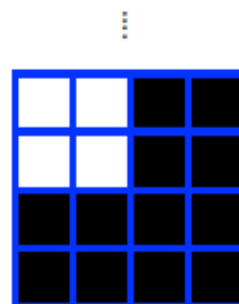


65 nm



2x4 cores @ 1.8 GHz  
(8 cores dark, 8 dim)

*(Industry's Choice)*



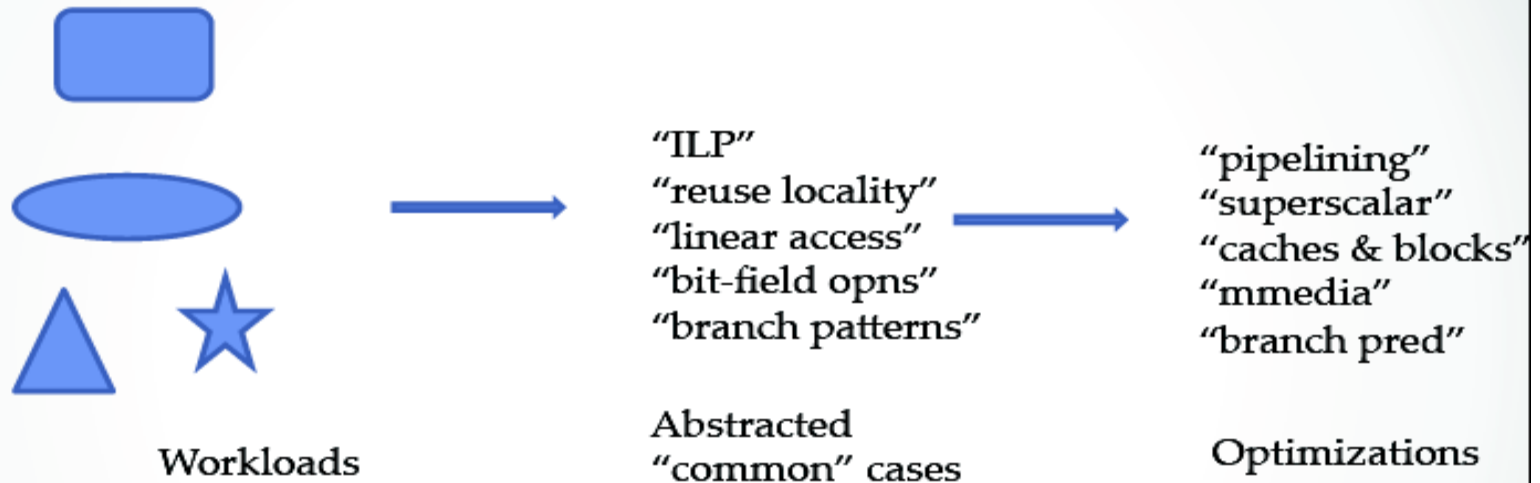
4 cores @ 2x1.8 GHz  
(12 cores dark)

*75% dark after 2 generations;  
93% dark after 4 generations*

32 nm

N. Goulding, J. Sampson, G. Venkatesh, S. Garcia,  
J. Auricchio, J. Babb, M. Taylor, and S. Swanson.  
“GreenDroid: A mobile application processor for a  
future of dark silicon.” In *HOTCHIPS*, 2010.

# Traditional Optimization: 90/10 Paradigm



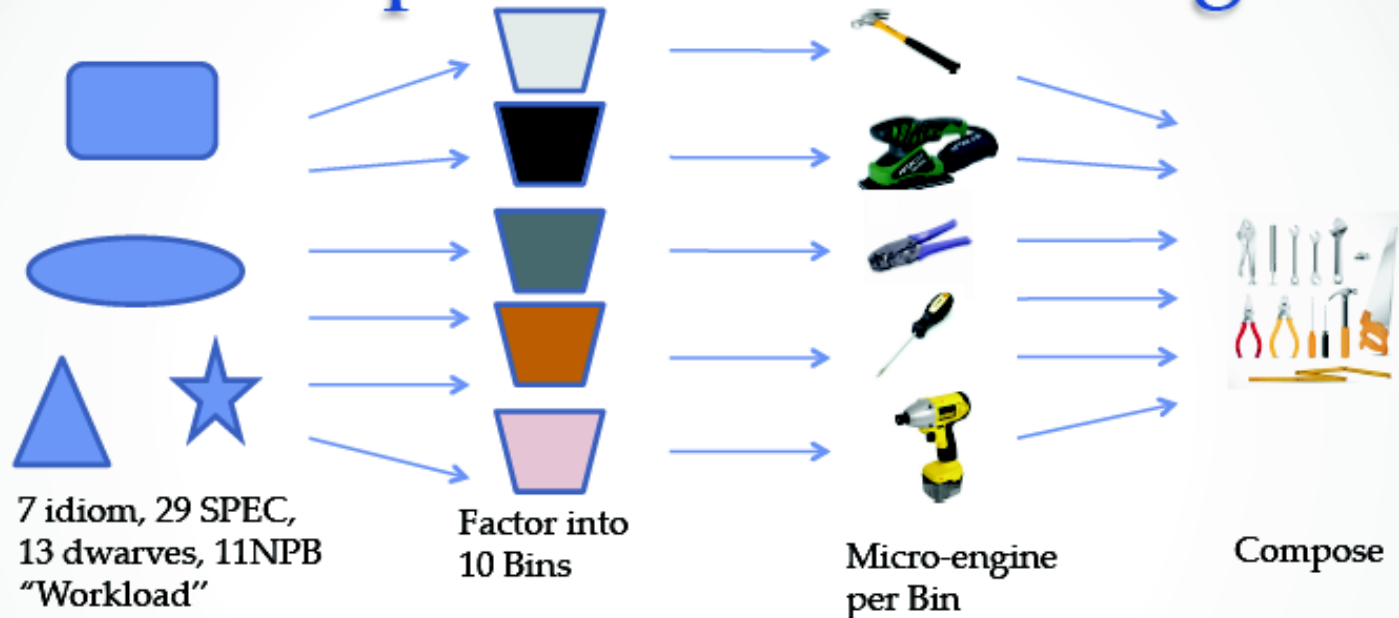
- Workloads: analyze and derive common cases(90%)
- Invent arch features, implementation optimizations with broad impact (90%)
- Improve performance by adding optimizations
- Aggregation and Efficiency: 8080 80 insts => SB 500+ instructions

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July 11, 2012

*Amdahl's Law, H&P's Comp Arch: A Quantitative Approach*

# 10x10 Optimization Paradigm

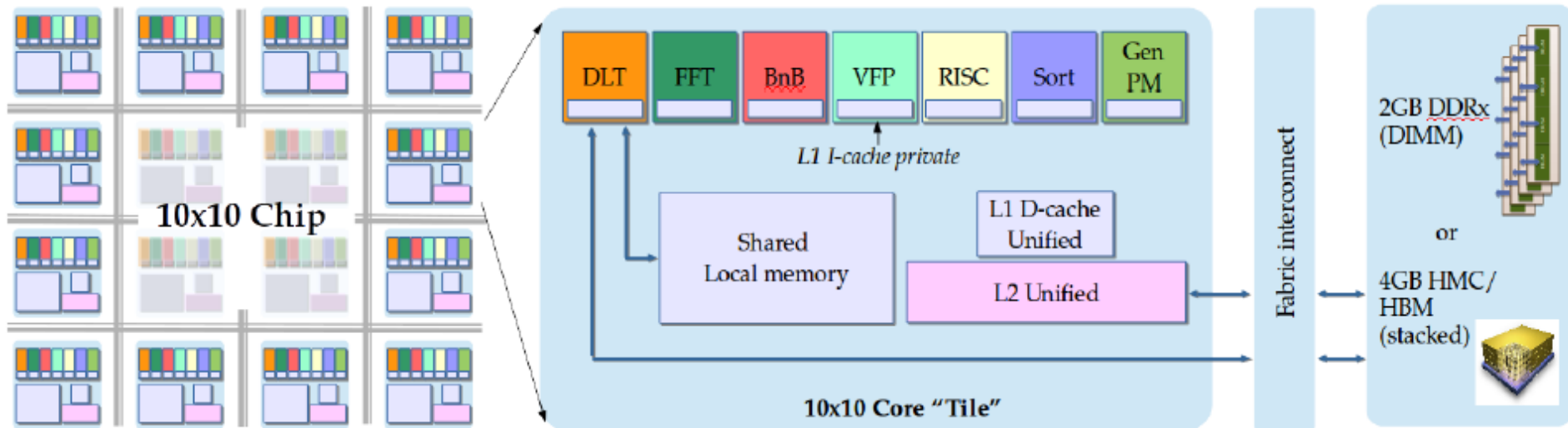


- Identify 10 application clusters; compute structures; datatypes (focus on 10 distinct bins)
- Optimize architecture, Optimize implementation of each separately (improve energy-delay product by 10-100x)
- Compose together sharing memory hierarchy and interconnect (preserve the benefits of customization)

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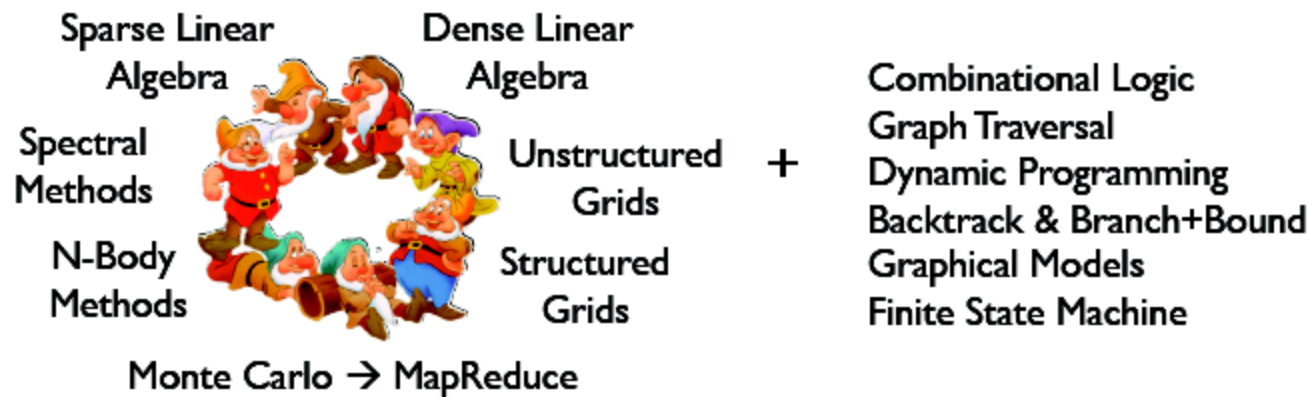
# 10x10 Architecture



10x10 Chip includes tiled 10x10 cores; each has several Micro-engines.

# What is OpenDwarf ?

- A (computational) dwarf is an algorithmic method that *captures a pattern of computation and communication*
  - Inspired by Phil Colella, who identified *seven* numerical methods important for science and engineering
- Benchmark Suite of 13 Computational Dwarfs & Apps



AMD Fusion Developer Summit, Bellevue, WA, USA, June 2011  
© W. Feng, 2011

# OpenCL synthesis on FPGA

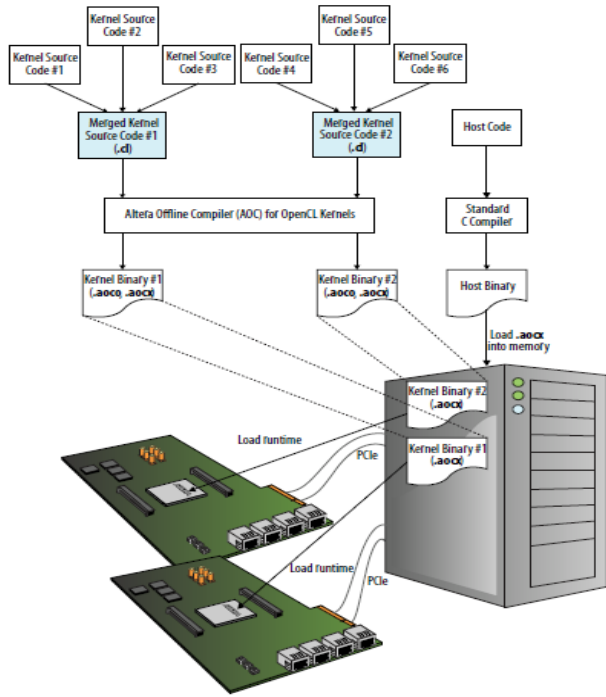


Table 1. Monte Carlo Black-Scholes Results

Platform	Power Watts (W)	Performance Simulations per second (Bsims/s)	Efficiency Simulations per second per Watt (Msims/s/W)
W3690 Xeon Processor	130	0.032	0.0025
nVidia Kepler20	212	10.1	48
BittWare S5-PCIe-HQ	45	12.0	266

- Pros
  - Customized Hardware
  - Better performance/Watt
- Cons
  - Large synthesis time



# FPGA Advantage

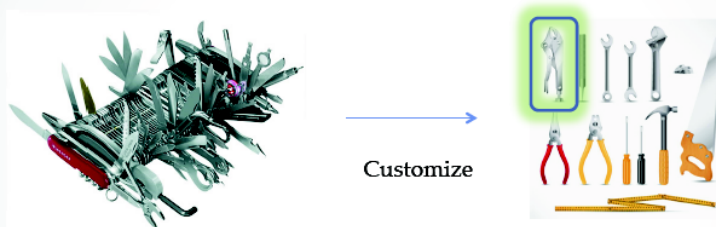
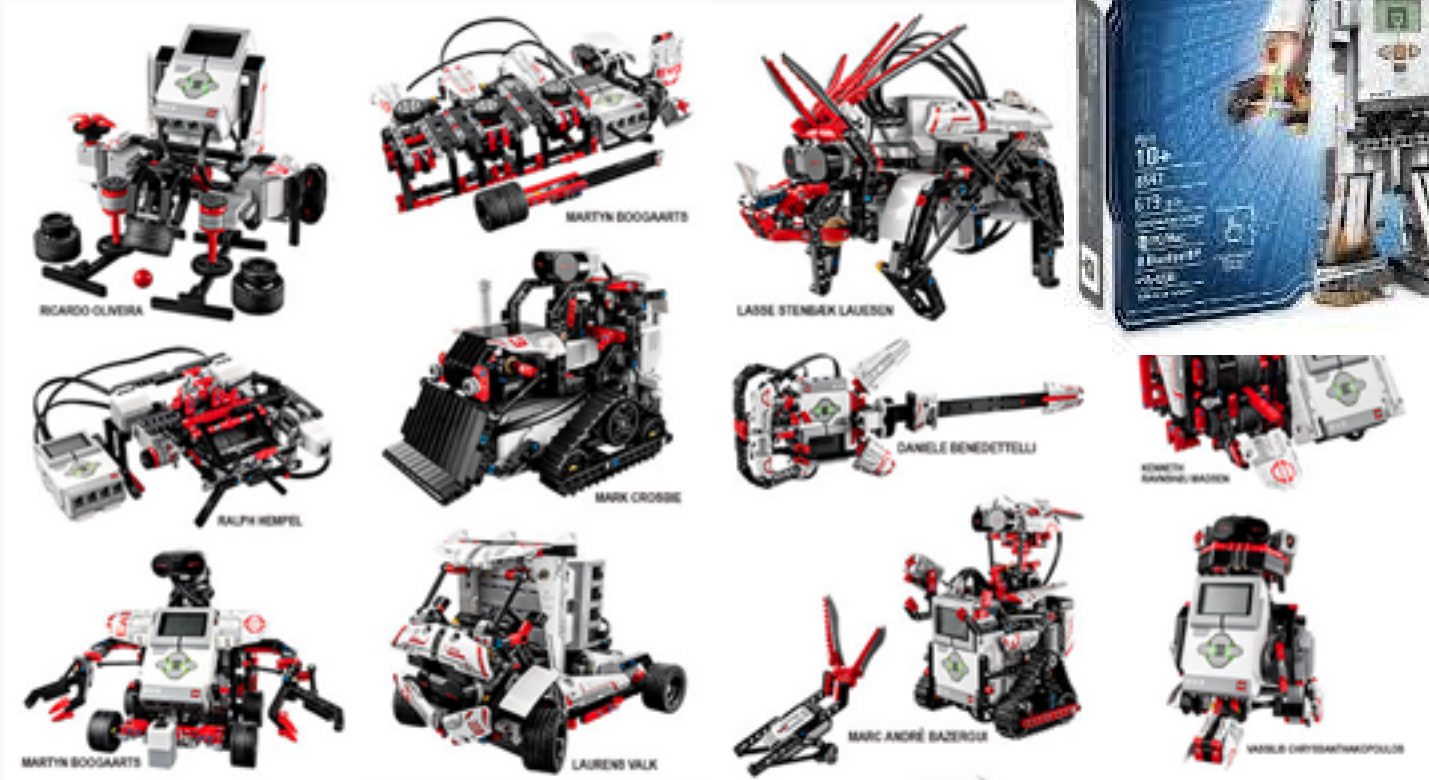
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[https://www.altera.com/en\\_US/pdfs/literature/wp/wp-01173-opencl.pdf](https://www.altera.com/en_US/pdfs/literature/wp/wp-01173-opencl.pdf)

# Refactoring OpenDwarfs



# Contribution

- Lower synthesis time for Kernels
- Improvement in performance/Watt
- Proving the concept on FPGA



Thank You